IN THE CLAIMS

1. (Currently Amended) A semiconductor device for comparing an input address with a stored repair address, comprising:

a signal controller for generating control signals including an enable signal;

an address latch unit in response to the control signals for latching the input address;

N number of M-bit address comparators, each enabled by the enable signal for comparing the input address with the stored repair address;

a comparator delay modeling block for delaying the ~~control~~ enable signal for a predetermined time; and

a repair circuit controller in response to ~~the~~ a delayed control signal output from the comparator delay modeling block for generating one of a repair address enable signal and a normal address enable signal based on a comparison result of an address comparator.

2. (Currently Amended) The semiconductor device as recited in claim 1, further comprising a comparator initialization unit for generating ~~an enable~~ a reset signal to enable and initialize ~~an~~ the N number of M-bit address comparators.

3. (Currently Amended) The semiconductor device as recited in claim 2, wherein each of the M-bit address comparators includes:

a fuse enabling means for ~~outputting a fuse enabling signal and~~ receiving the ~~fuse enabling~~ reset signal to output a fuse enable signal in response to whether an enabling fuse included in the fuse enabling means is blown out or not;

a plurality of unit repair address comparing means for respectively comparing each bit of the input address which is latched in the address latching means with each bit of the stored repair address which is stored in the repair address comparing means; and

a signal combination means for outputting ~~the~~ a repair signal in response to results of the plurality of unit repair address comparing means,

wherein the signal combination means is enabled by the fuse enabling signal.

4. (Original) The semiconductor device as recited in claim 3, the fuse enabling means includes:

a first MOS transistor connected to a supply voltage, gates of the first MOS transistor being supplied with a fuse reset signal;

a second MOS transistor connected to a ground voltage, gates of the second MOS transistor being supplied with the fuse reset signal;

an enabling fuse coupled between the first and second MOS transistors;

a first inverter for receiving a signal supplied between the enable fuse and the second MOS transistor;

a third MOS transistor connected between an input terminal of the first inverter and the ground voltage, gate of the third MOS transistor being coupled to an output terminal of the first inverter;

a second inverter for receiving an outputted signal from the first inverter;

a first transmission gate for outputting the enabling signal as the fuse enabling signal by turning on in case when the enable fuse is blown out; and

a second transmission gate for outputting the supplied signal between the enable fuse and the second MOS transistor as the fuse enabling signal by turning on in case when the enable fuse is not blown out,

wherein the first and the second transmission gates are controlled by outputted signals from the first and the second inverters.

5. (Original) The semiconductor device as recited in claim 4, the fuse enabling means further includes a delay means for delaying the enabling signal for a predetermined time, i.e., delay value of the latched address.

6. (Original) The semiconductor device as recited in claim 5, the unit repair address comparing means includes:

a forth MOS transistor connected to a supply voltage, gates of the forth MOS transistor being supplied with a fuse reset signal;

a fifth MOS transistor connected to a ground voltage, gates of the fifth MOS transistor being supplied with the fuse reset signal;

an address fuse coupled between the forth and fifth MOS transistors;

a third inverter for receiving a signal supplied between the address fuse and

the fifth MOS transistor;

a sixth MOS transistor connected between an input terminal of the third inverter and the ground voltage, gate of the sixth MOS transistor being coupled to an output terminal of the third inverter;

a forth inverter for receiving an outputted signal from the first inverter;

a third transition gate for outputting one bit of the inputted address to the signal combination means as a comparison signal by turning on if the address fuse is blown out; and

a forth transition gate for outputting one bit of the inverse inputted address to the signal combination means as a comparison signal by turning on if the address fuse is not blown out.

7. (Original) The semiconductor device as recited in claim 6, the signal combination means includes:

a plurality of first NOR gates for receiving the fuse enabling signal and the comparison signal outputted from the plurality of unit repair address comparing means;

a plurality of first NAND gates for receiving outputted signals from the plurality of first NOR gates;

a second NOR gate for receiving outputted signals from the plurality of first NAND gates; and

a fifth inverter for receiving an outputted signal from the second NOR gate and outputting the repair signal.

8. (Original) The semiconductor device as recited in claim 7, the repair address comparison replica includes:

a third NOR gate for delaying the enabling signal by a delay time of the comparison signal outputted from the plurality of unit repair address comparing means by delaying value of the plurality of first NOR gate;

a second NAND gate for delaying an outputted signal from the third NOR gate by a delay time of the plurality of first NOR gate; and

a forth NOR gate for delaying an outputted signal from the second NAND gate by a delay time of the second NOR gate.

9. (Original) The semiconductor device as recited in claim 8, the repair address comparison replica further includes an output controller for adjusting phase and level of an outputted signal from the forth NOR gate in order to equalizing phase and level of an outputted signal from the forth NOR gate with phase and level of the repair signal which is delivered from the repair address comparing means to the repair circuit controller.

10. (Original) The semiconductor device as recited in claim 3, the fuse enabling means includes:

a first MOS transistor connected to a supply voltage, gates of the first MOS transistor being supplied with a fuse reset signal;

a second MOS transistor connected to a ground voltage, gates of the second MOS transistor being supplied with the fuse reset signal;

an enabling fuse coupled between the first and second MOS transistors;

a first inverter for receiving a signal supplied between the enable fuse and the second MOS transistor;

a third MOS transistor connected between an input terminal of the first inverter and the ground voltage, gate of the third MOS transistor being coupled to an output terminal of the first inverter; and

a first NAND gate for receiving the enabling signal and an outputted signal from the first inverter and outputting the fuse enabling signal.

11. (Original) The semiconductor device as recited in claim 10, the signal combination means includes:

a plurality of first NOR gates for receiving the fuse enabling signal and the comparison signal outputted from the plurality of unit repair address comparing means;

a plurality of second NAND gates for receiving outputted signals from the plurality of first NOR gates;

a second NOR gate for receiving outputted signals from the plurality of second NAND gates; and

a second inverter for receiving an outputted signal from the second NOR

gate and outputting the repair signal.

12. (Original) The semiconductor device as recited in claim 11, the repair address comparison replica includes:

a third inverter for receiving the enabling signal;

a third NOR gate for delaying the comparison signal outputted from the plurality of unit repair address comparing means by a delay value of the plurality of first NOR gate;

a second NAND gate for delaying an outputted signal from the third NOR gate by a delay value of the plurality of first NOR gate; and

a forth NOR gate for delaying an outputted signal from the second NAND gate by a delay value of the second NOR gate.

13. (Original) The semiconductor device as recited in claim 12, the repair address comparison replica further includes an output controller for adjusting phase and level of an outputted signal from the forth NOR gate in order to equalizing phase and level of an outputted signal from the forth NOR gate with phase and level of the repair signal which is delivered from the repair address comparing means to the repair circuit controller.

14. (Original) The semiconductor device as recited in claim 1, the repair circuit controller includes:

at least one repair signal combination means for receiving the plurality of repair signals which is outputted from the plurality of repair address comparing means and driving level of the repair sensing node in response to result of combining the plurality of repair signals;

a repair signal path replica for delaying the enabling signal which passes through the repair address comparison replica for delay value until the repair signal combination means drives the level of the repair sensing node since the repair signal combination means receives the plurality of repair signals;

a first output means for outputting a redundancy circuit enabling signal which is used for operating the redundancy circuit in response to the level of the repair sensing node; and

a second output means for outputting a normal circuit enabling signal which is used for operating the normal circuit in response to the level of the repair sensing node after enabled by the enabling signal which passes through the repair signal path replica.

15. (Original) The semiconductor device as recited in claim 14, the repair signal combination means includes:

a plurality of first NAND gates for receiving the plurality of repair signals;

a plurality of first NOR gates for receiving outputted signals from the plurality of first NAND gates; and

at least one second NAND gate for receiving outputted signals from the plurality of first NOR gates and driving the level of repair sensing node.

16. (Original) The semiconductor device as recited in claim 15, the repair signal path replica includes:

a third NAND gate for delaying the enabling signal which passes through the repair address comparison replica for delay value of the first NAND gate;

a second NOR gate for delaying an outputted signal from the third NAND gate for delay value of the first NOR gate; and

a forth NAND gate for delaying an outputted signal from the second NOR gate for delay value of the second NAND gate.

17. (Original) The semiconductor device as recited in claim 16, the repair signal path replica further includes an output controller for adjusting phase and level of an outputted signal from the forth NAND gate in order to equalizing phase and level of the repair sensing node.

18. (Original) The semiconductor device as recited in claim 17, the second output means includes:

a fifth NOR gate for receiving the level of the repair sensing node and the enabling signal which is outputted from the repair signal path replica; and

a buffer for buffering an output signal of the fifth NOR gate and outputting the normal circuit enabling signal.

19. (New) A semiconductor device for comparing an input address with a stored repair address, comprising:

a signal controller for generating control signals;

an address latch unit in response to at least one of the control signals for latching the input address;

N number of M-bit address comparators, each for comparing the input address with the stored repair address;

a comparator delay modeling block for delaying one of the control signals for a predetermined time;

a repair circuit controller in response to a delayed control signal output from the comparator delay modeling block for generating one of a repair address enable signal and a normal address enable signal based on a comparison result of an address comparator; and

a comparator initialization unit for initializing the N number of M-bit address comparators.

20. (New) The semiconductor device as recited in claim 19, wherein the comparator initialization unit generates a reset signal to enable the N number of M-bit address comparators.